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EXAMINER	
O'BRIEN, BARRY J	

ART UNIT	PAPER NUMBER
2183	5

DATE MAILED: 12/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,377	JARVIS, ANTHONY X.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/29/00, 4/16/01, and 7/16/02*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-20 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Declaration Fee as received on 4/16/2001 and IDS as received on 7/16/2002.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

4. Claim 11 is objected to because of the following informalities:

   a. Regarding claim 11, please arrange the claimed elements in a logical order. Specifically, the indented features of the "data processor" should be located under the element "data processor", rather than under the element "a plurality of memory-mapped peripheral circuits".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakanishi, U.S. Patent No. 5,805,852.

7. Regarding claim 1, Nakanishi has taught a data processor comprising:

a. An instruction execution pipeline comprising:

i. A read stage ("MEM" stage, see Col.9 lines 13-23),

ii. A write stage ("WB" stage, see Col.9 lines 13-23),

iii. A first execution stage ("EX" stage, see Col.9 lines 13-23) comprising E execution units capable of producing data results from data operands (see "EX" stages of 7-1 through 7-4 of Fig.1, and Col.10 lines 1-5),

b. A register file (5 of Fig.1) comprising a plurality of data registers, each of said data registers capable of being read by said read stage of said instruction pipeline (see Col.9 lines 53-56) via at least one of R read ports of said register file (see Col.9 lines 5-9) and each of said data registers capable of being written by said write stage of said instruction pipeline (see Col.9 lines 61-64) via at least one of W write ports of said register file (see Col.9 lines 5-9),

c. Bypass circuitry capable of receiving data results from output channels of source devices in at least one of said write stage and said first execution stage, said bypass circuitry comprising a first plurality of bypass tri-state line drivers having input channels coupled to first output channels of a first plurality of said source devices and tri-state output channels coupled to a first common read data channel in said read stage (see Fig.3, Col.10 lines 61-67 and Col.11 lines 16-32).

8. Regarding claim 2, Nakanishi has taught the data processor as set forth in claim 1 above, wherein said bypass circuitry further comprises a second plurality of bypass tri-state line drivers having input channels coupled to said first output channels of said first plurality of said source devices and tri-state output channels coupled to a second common read data channel in said read stage (see Fig.3, Col.10 lines 61-67 and Col.11 lines 16-32).

9. Regarding claim 3, Nakanishi has taught the data processor as set forth in claim 2 above, further comprising a first register file tri-state line driver having an input channel coupled to a first one of said R read ports and an output channel coupled to said first common read data channel in said read stage (see Fig.3, and Col.10 lines 48-60).

10. Regarding claim 4, Nakanishi has taught the data processor as set forth in claim 3 above, further comprising a second register file tri-state line driver having an input channel coupled to a second one of said R read ports and an output channel coupled to said second common read data channel in said read stage (see Fig.3, and Col.10 lines 48-60).

11. Regarding claim 5, Nakanishi has taught the data processor as set forth in claim 4 above, further comprising a first multiplexer having a first input channel coupled to said first common read data channel and an output channel coupled to a first operand channel of a first execution

unit in said first execution stage (see Fig.3 and Col. 10 lines 11-60). Here, the tri-state network of Fig.3 performs the same function as the multiplexer, choosing between data being input from the register file and data bypassed from the EX or MEM stages.

12. Regarding claim 6, Nakanishi has taught the data processor as set forth in claim 5 above, further comprising a second multiplexer having a first input channel coupled to said second common read data channel and an output channel coupled to a second operand channel of said first execution unit in said first execution stage (see Fig.3 and Col. 10 lines 11-60). Here, the tri-state network of Fig.3 performs the same function as the multiplexer, choosing between data being input from the register file and data bypassed from the EX or MEM stages.

13. Regarding claim 7, Nakanishi has taught the data processor as set forth in claim 6 above, wherein said bypass circuitry comprises a first bypass channel coupling an output channel of said first execution unit to a second input channel of said first multiplexer (see Fig.3 and Col.10 lines 11-60). Again, here the tri-state network of Fig.3 performs the same function as a multiplexer, choosing between data being input from the register file and data bypassed from the EX or MEM stages.

14. Regarding claim 8, Nakanishi has taught the data processor as set forth in claim 7 above, wherein said first bypass channel couples said output channel of said first execution unit to a second input channel of said second multiplexer (see Fig.3 and Col.10 lines 11-60). Again, here the tri-state network of Fig.3 performs the same function as multiplexer, choosing between data being input from the register file and data bypassed from the EX or MEM stages.

15. Regarding claim 9, Nakanishi has taught the data processor as set forth in claim 8 above, wherein said bypass circuitry further comprises a second bypass channel coupling an output

channel of a second execution unit in said first execution stage to a third input channel of said first multiplexer (see Fig.3 and Col.10 lines 11-60). Here, Fig.3 shows the multiple execution units in the execution stage that are also bypassed back through the tri-state network, which performs the same function as multiple multiplexers. Also, Col.10 lines 11-60 has taught each execution unit in the EX stage allowing data to be bypassed to each of the other execution units in the EX stage via the tri-state network, thus creating the a multiplexed data path from a second execution unit to a first execution unit as claimed.

16. Regarding claim 10, Nakanishi has taught the data processor as set forth in claim 9 above, wherein said second bypass channel couples said output channel of said second execution unit to a third input channel of said second multiplexer (see Fig.3 and Col.10 lines 11-60). Here, Fig.3 shows the multiple execution units in the execution stage that are also bypassed back through the tri-state network, which performs the same function as multiple multiplexers. Also, Col.10 lines 11-60 has taught each execution unit in the EX stage allowing data to be bypassed to each of the other execution units in the EX stage via the tri-state network, thus creating the a multiplexed data path from a second execution unit to a first execution unit as claimed.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 11-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi, U.S. Patent No. 5,805,852, in further view of Ferris, III et al., U.S. Patent No. 4,591,973.

19. Regarding claims 11, Nakanishi has taught a processing system comprising:

a. A data processor (see Fig.1),

b. A memory coupled to said data processor (1 of Fig.1),

c. Wherein said data processor comprises:

I. An instruction execution pipeline comprising:

i. A read stage ("MEM" stage, see Col.9 lines 13-23),

ii. A write stage ("WB" stage, see Col.9 lines 13-23),

iii. A first execution stage ("EX" stage, see Col.9 lines 13-23) comprising E execution units capable of producing data results from data operands (see "EX" stages of 7-1 through 7-4 of Fig.1, and Col.10 lines 1-5),

II. A register file (5 of Fig.1) comprising a plurality of data registers, each of said data registers capable of being read by said read stage of said instruction pipeline (see Col.9 lines 53-56) via at least one of R read ports of said register file (see Col.9 lines 5-9) and each of said data registers capable of being written by said write stage of said instruction pipeline (see Col.9 lines 61-64) via at least one of W write ports of said register file (see Col.9 lines 5-9),

III. Bypass circuitry capable of receiving data results from output channels of source devices in at least one of said write stage and said first execution

stage, said bypass circuitry comprising a first plurality of bypass tristate line drivers having input channels coupled to first output channels of a first plurality of said source devices and tristate output channels coupled to a first common read data channel in said read stage (see Fig.3, Col.10 lines 61-67 and Col.11 lines 16-32).

20. Nakanishi has not explicitly taught a plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor.

21. However, Ferris has taught a plurality of memory-mapped peripheral circuits coupled to a data processor (see Fig.1, Col.1 lines 43-52, and Col.3 lines 3-19) in order to decrease the burden on the main processor and provide greater throughput and performance (see Col.1 lines 21-31). One of ordinary skill in the art would have recognized that increasing the performance of microprocessor systems is a primary goal of their designers. Therefore, one of ordinary skill in the art would have found it obvious to modify Nakanishi to include a plurality of memory-mapped peripheral circuits in order to increase the performance of the processor (see Col.1 lines 21-31).

22. Regarding claim 12, Nakanishi has taught the processing system as set forth in claim 11 above, wherein said bypass circuitry further comprises a second plurality of bypass tristate line drivers having input channels coupled to said first output channels of said first plurality of said source devices and tristate output channels coupled to a second common read data channel in said read stage (see Fig.3, Col.10 lines 61-67 and Col.11 lines 16-32).

23. Regarding claim 13, Nakanishi has taught the processing system as set forth in claim 12 above, further comprising a first register file tristate line driver having an input channel coupled to a first one of said R read ports and an output channel coupled to said first common read data channel in said read stage (see Fig.3, and Col.10 lines 48-60).

24. Regarding claim 14, Nakanishi has taught the processing system as set forth in claim 13 above, further comprising a second register file tristate line driver having an input channel coupled to a second one of said R read ports and an output channel coupled to said second common read data channel in said read stage (see Fig.3, and Col.10 lines 48-60).

25. Regarding claim 15, Nakanishi has taught the processing system as set forth in claim 14 above, further comprising a first multiplexer having a first input channel coupled to said first common read data channel and an output channel coupled to a first operand channel of a first execution unit in said first execution stage (see Fig.3 and Col. 10 lines 11-60). Here, the tri-state network of Fig.3 performs the same function as the multiplexer, choosing between data being input from the register file and data bypassed from the EX or MEM stages.

26. Regarding claim 16, Nakanishi has taught the processing system as set forth in claim 15 above, further comprising a second multiplexer having a first input channel coupled to said second common read data channel and an output channel coupled to a second operand channel of said first execution unit in said first execution stage (see Fig.3 and Col. 10 lines 11-60). Here, the tri-state network of Fig.3 performs the same function as the multiplexer, choosing between data being input from the register file and data bypassed from the EX or MEM stages.

27. Regarding claim 17, Nakanishi has taught the processing system as set forth in claim 16 above, wherein said bypass circuitry comprises a first bypass channel coupling an output channel

of said first execution unit to a second input channel of said first multiplexer (see Fig.3 and Col.10 lines 11-60). Again, here the tri-state network of Fig.3 performs the same function as a multiplexer, choosing between data being input from the register file and data bypassed from the EX or MEM stages.

28. Regarding claim 18, Nakanishi has taught the processing system as set forth in claim 17 above, wherein said first bypass channel couples said output channel of said first execution unit to a second input channel of said second multiplexer (see Fig.3 and Col.10 lines 11-60). Again, here the tri-state network of Fig.3 performs the same function as multiplexer, choosing between data being input from the register file and data bypassed from the EX or MEM stages.

29. Regarding claim 19, Nakanishi has taught the processing system as set forth in claim 18 above, wherein said bypass circuitry further comprises a second bypass channel coupling an output channel of a second execution unit in said first execution stage to a third input channel of said first multiplexer (see Fig.3 and Col.10 lines 11-60). Here, Fig.3 shows the multiple execution units in the execution stage that are also bypassed back through the tri-state network, which performs the same function as multiple multiplexers. Also, Col.10 lines 11-60 has taught each execution unit in the EX stage allowing data to be bypassed to each of the other execution units in the EX stage via the tri-state network, thus creating the a multiplexed data path from a second execution unit to a first execution unit as claimed.

30. Regarding claim 20, Nakanishi has taught the processing system as set forth in claim 19 above, wherein said second bypass channel couples said output channel of said second execution unit to a third input channel of said second multiplexer (see Fig.3 and Col.10 lines 11-60). Here, Fig.3 shows the multiple execution units in the execution stage that are also bypassed back

through the tri-state network, which performs the same function as multiple multiplexers. Also, Col.10 lines 11-60 has taught each execution unit in the EX stage allowing data to be bypassed to each of the other execution units in the EX stage via the tri-state network, thus creating the a multiplexed data path from a second execution unit to a first execution unit as claimed.

Conclusion

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

32. Wechsler, U.S. Patent No. 5,764,943, has taught a processor which allows the results of an execution stage to be bypassed to the read stage of a subsequent instruction on a tri-state bus.

33. Kawasaki, U.S. Patent No. 5,467,476, has taught a processor which has bypass circuitry for transferring the result of an execution between multiple execution pipelines without being written to the register file.

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 7am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
12/5/2003

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